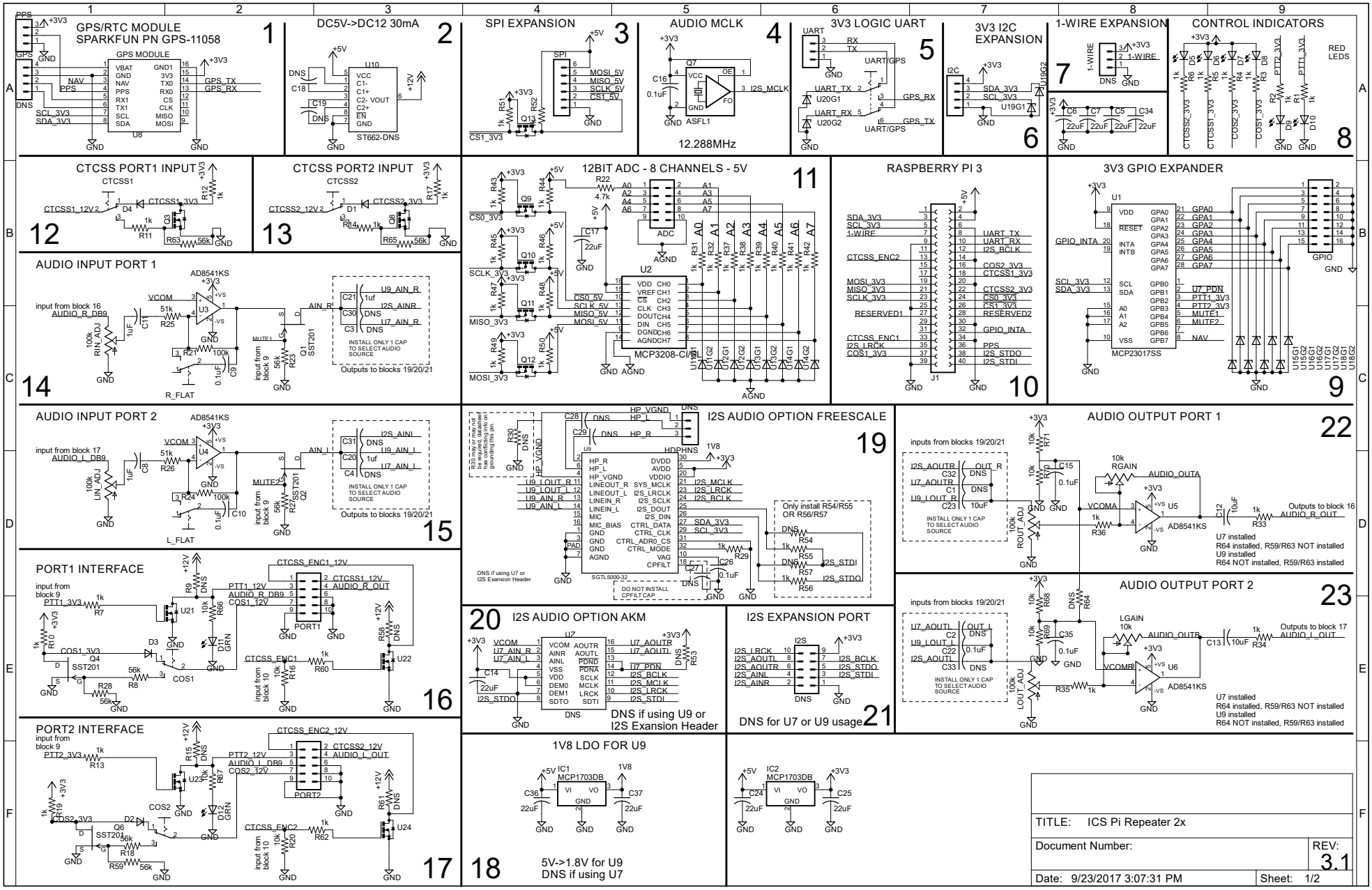
GPS/RTC MODULE
SPARKFUN PN GPS-11058
DC5V->DC12 30mA
SPI EXPANSION
AUDIO MCLK
12.288MHz
3V3 LOGIC UART
3V3 I2C EXPANSION
1-WIRE EXPANSION
CONTROL INDICATORS
CTCSS PORT1 INPUT
CTCSS PORT2 INPUT
12BIT ADC - 8 CHANNELS - 5V
RASPBERRY PI 3
3V3 GPIO EXPANDER
AUDIO INPUT PORT 1
AUDIO INPUT PORT 2
I2S AUDIO OPTION FREESCALE
AUDIO OUTPUT PORT 1
AUDIO OUTPUT PORT 2
PORT1 INTERFACE
PORT2 INTERFACE
I2S AUDIO OPTION AKM
I2S EXPANSION PORT
1V8 LDO FOR U9
DNS if using U9 or I2S Exansion Header
DNS for U7 or U9 usage
5V->1.8V for U9
DNS if using U7
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BASIC THEORY OF OPERATION

BLOCK 1: GPS MODULE

The GPS module is an Off The Shelf GPS solution with an external antenna (sold seperately) designed and sold by SparkFun Electronics. This unit will dock with this design for users who wish to have have an RTC that is syncronized to GPS time.

BLOCK 2: 5Vdc -> 12Vdc @ 30mA

12v is used by only a few pull-up components in this design so current is limited. These pull-ups will only be useful for radios that do not have internal pull ups on the external PTT and CTCSS Encode circuits.

BLOCK 3: 5V SPI BUS EXPANSION

A SPI bus header is provided to allow for expansion of a single 5.0Vdc SPI protocol device. The signals are buffered by a FET logic shifter to provide limited protection from ESD and overvoltage conditions.

BLOCK 4: AUDIO MCLK

This block is to provide the master clock need by the audio codec chips as the PI platform cannot provide this clock to the chips natively.

BLOCK 5: 3V3 LOGIC UART

This block provides a 3V3 logic level uart connection directly to the PI platform for debug use in case user does not have ethernet access, or wishes to use the GPS modules utilizes uart protocol for timing messages. These pins have a zener diode on the lines for limited protection against ESD and overvoltage.

For GPS usage, the switch must be moved to the GPS location which will disconnect the header from the PI device.

BLOCK 6: 3V3 I2C EXPANSION

This block provides a 3V3 logic level uart connection directly to the PI platform for debug use in case user does not have ethernet access, or wishes to use the GPS modules utilizes uart protocol for timing messages. These pins have a zener diode on the lines for limited protection against ESD and overvoltage conditions.

For GPS usage, the switch must be moved to the GPS location which will disconnect the header from the PI device.

BLOCK 7: 1-WIRE EXPANSION

This port is provided to allow the user to utilize a 3V3 1-wire device, or expose the user clock source for external usages. This pin is connected directly to the PI with NO PROTECTION. The user must handle all circuit protection needs related to this circuit.

BLOCK 8: LED INDICATORS

The indicators are wired for active low signal conditions due to the input management circuits. When monitoring these signals, it is important toremember the input management circuits will always output an active low signal to the processor regardless of the actual active state provided by the radio. This is discussed further in BLOCK 12/13.

BLOCK 9: GPIO EXPANDER

A 16 BIT (2x8bit banks) is used to provide user accessible GPIO pins while still providing a layer of protection to the processor. Eight of the pins are exposed to the user and include a zener diode protection circuit for some limited protection of the device from ESD and overvoltage conditions. The GPIO are capable of driving or receiveing 3V3 TTL signals and may be configured on a pin by pin basis. Internal pull-ups are available on all pins if configured.

BLOCK 10: PI3 INTERFACE

2x20 Stacking Header for interconnecting with the PI3 header.

BLOCK 11: 8 CHANNEL 5V ADC

This block provides the user 8 channels of 12-bit ADC inputs with 5V capability. All channels are independantly current limited and zener protected to help prevent damage. It is upon the user to configure each channel in the OpenRepeater GUI for their specific applications.

BLOCK 12/13: CTCSS INPUTS

As the CTCSS input signals are 12V and may be either active HIGH or LOW, this circuit converts the signal to a 3V3 ACTIVE LOW input to the PI.
*With an active HIGH input, the input should be fed to the FET gate, which will turn on the FET, pulling the PI input to ground.
*With an active LOW input, the input should be fed to the diode, which will forward bias the diode, pulling the PI input to ground.

BLOCK 14/15: AUDIO INPUTS

This unit is designed to accept 1 channel each of mono input from the radios on port 1 and 2. A multi turn pot is used for input level adjust. Coming out of the pot, the signal is fed into an buffer amplifier which has an optional switch to convert to flat audio.
After the buffer amplifier is a JFET which can be used to mute the channel temporarily when the system is configured for blended audio. This is useful to shut down an interference or malfunctioning audio source without having to reconfigure the system.
After the amplifier is a 3-way fork of the audio, this will normally only be populated with a single capacitor based on the audio codec being used in the system.

BLOCK 16/17: RADIO INTERFACES

A 2x5 header and circuitry to interface with the radio
* PTT/CTCSS Encode is output as a 3V3 signal but act on a 12V signal to the radio the radio, so this signal is opto-isolated to the radio.
*COS is received from the radio as a 12V signal so is protected and converted to an active LOW signal into the microcontroller.
See Block 12/13 description for more detailed explanation of the circuitry behavior.

BLOCK 18: 1V8 LDO REGULATOR

A simple regulator for providing the 1.8V required to power U9 CODEC. If U7 or the external I2S codec are used this part can be ommitted.

BLOCK 19-21: I2S AUDIO CODECS

The design includes options for an AK4554VT as well as a SGTL5000, and also has provisions for a third external user designed audio codec interface. Only a single I2S device may installed on the hardware bus, if using the expander circuit, the ICS at U7 and U9 must be removed from the board and the appropriate capacitors relocated in blocks 14/15/22/23 to select the expansion header.

BLOCK 22/23: AUDIO OUTPUTS

Similar to the input circuits, these blocks have a capacitor fork for selecting the source of the audio to receive into the output stages. After the audio source selection capacitors is a level adjust potentiometer followed by an amplifier stage with a potentiometer for gain adjust. Following the amplifiers is a RC section for load impedace matching.

Due to the nature of the codecs, some output a common voltage while others do not. To handle this condition R59/R63/R64 are used to either bridge the common inputs (R64) or adjust individually the channels (R59/R63) for best amplifier centering.

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